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ARTICLE

Performance evaluation of a 15-level inverter using two DC sources with lower standing voltage

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ABSTRACT

Most of the reduced switch multilevel inverters (MLIs), including switched capacitor MLIs (SC-MLIs), are designed with voltage sources/capacitors have obtained voltage levels with the addition of these sources only. This increases the number of voltage sources (capacitors) without full utilisation of these sources and has higher inverter total standing voltages, which leads the inverter inefficient (high conduction loss) and costly. The motivation of this work is to design a generalised reduced component MLI aiming for addition as well as subtraction of the voltage sources to obtain a voltage level, which results in the reduction of sources, enhance the voltage utilisation and lowering the inverter total standing voltage (TSV). The design parameters of the proposed MLI topology are compared with the recently developed MLIs in terms of the number of switches, capacitors and TSV to prove its superiority. The experimental prototype of the specimen 15-level and 27-level inverters is implemented using DS1103 and the corresponding results are presented.

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KEYWORDS
Multi-level inverters; total standing voltage (TSV); cost function; components cost

1. Introduction

Multi-level inverters (MLIs) have been overpowered the two-level inverters due to its important features over the conventional inverter like lower voltage stresses on the switches, better harmonic profiles and smaller filter requirements (Rodriguez et al., 2002). Therefore, the MLIs have been used in various applications like FACTS devices, traction drives, grid interfacing with the photo-voltaic system (Sinha et al., 2018), HVDC, several industrial applications (pumps, conveyers, fans, blowers), etc. The classical inverters like cascaded H-bridge (CHB) inverter (Baker, 1980), neutral point clamped (NPC) inverter (Nabae et al., 1980) and flying capacitor (FC) type (Dargahi & Corzine, 2015) MLIs have solved most of the limitations observed in the two-level inverters. The NPC and FC inverters necessitate low-voltage-rated switches in combination with a single DC

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voltage source of higher magnitude aiming to the sinusoidal waveform for better power quality output voltage. However, they are limited to 3-level to 5-level only due to the requirement of a complex capacitor voltage balancing technique. On the other hand, CHB inverter has a very large number of conducting switches, which increases the losses of the inverter. Moreover, the inverter requires several isolated voltage sources that increase the overall cost of the system. Recently, several reduced components MLIs have been developed that can be classified as the reduced switch-based MLIs and reduced source-based MLIs. Most of the reduced switch MLIs (Gautam, 2018; Majumdar et al., 2020; Samadaei & Adabi, 2018, Mahato et al., 2019) have overcome most of the problems associated with conventional MLIs. However, problems like the use of a greater number of asymmetrical DC sources in an inverter increase the size and cost of the MLIs. To overcome the abovementioned problems, switched capacitor MLIs (SC-MLI) have been developed very recently. The SC-MLIs (Arun & Noel, 2018; Babaei & Gowgani, 2014; Gautam, 2018; Khan et al., 2020; Khenar et al., 2018; Pal et al., 2022; Ramaiah et al., 2019; Saeedian et al., 2019; Samadaei et al., 2019; Taghvaie et al., 2017) are designed to replace most of the isolated DC sources to electrolytic capacitors so that the inverter can be designed with minimum cost and will be compact.

The topology depicted in Samadaei and Adabi (2018) uses 12 switches and four DC sources to produce 17 voltage levels of bipolar nature. However, the numbers of DC sources in the MLI are comparatively more and the voltage levels are obtained by the addition of voltage sources only, which results in larger inverter total standing voltage (TSV). A switched-capacitor MLI (SC-MLI) (Gautam, 2018) is proposed, which is a cascade connection of two T-type modules with some additional switches for capacitors balancing. But, the total standing voltage (TSV) is comparatively higher due to the addition of H-bridges. The inverter proposed in Arun and Noel (2018) is a cross-connected T-type module where switches are replaced by extra diodes. Due to the absence of any extra H-bridge circuit, the inverter TSV is comparatively lower. The configuration (Saeedian et al., 2019) uses two half-bridges at either side of the input DC sources for generating voltage levels. The switched-capacitor units are connected in cascade in the middle of the module to boost up the voltage levels for medium/high voltage applications using a single DC source. Similarly, the topology (Taghvaie et al., 2017) has no polarity reversal structure has lower TSV. A kite-type (K-Type) inverter (Samadaei et al., 2019) that designed with two asymmetrical DC sources and two asymmetrical capacitors to obtain 13 voltage levels. However, the number of bi-directional switches is more. In addition, the hybrid topology (Gautam, 2018) constitutes fault-tolerant capability due to the presence of redundancies in switching states. However, due to the presence of four additional switches attached to an individual unit, it offers maximum blocking voltage across them. Therefore, the TSV is high for the cascade connection. An inverter topology is presented in Pal et al. (2022) that can boost up the voltage levels in a trinary asymmetrical manner with lower TSV and cost function. The topology (Majumdar et al., 2020) arranges the voltage sources in trinary order and the addition and subtraction of DC sources are utilised for more voltage level generation. But the TSV is high due to the presence of an extra H-bridge circuit for their polarity generation. A seven-level SC-MLI (Khan et al., 2020) is proposed for a grid-connected system, in which the voltage across capacitors is self-balanced. Another SC topology (Babaei & Gowgani, 2014) is presented where extra H-bridge is used for polarity reversal and hence has higher TSV. A recent SC-MLI

configuration (Khenar et al., 2018) is discussed that uses T-type and cross-connected modules to generate a multi-level ac waveform. However, the TSV is comparatively higher because of the additional switches used for capacitor charging/discharging as well for level generation. A multi-sourced SC-MLI is presented in Ramaiah et al. (2019), in which the equal numbers of input DC sources and capacitors are used for a given output voltage. A mathematical expression on the capacitor energy utilisation factor is derived to determine the efficiency of the capacitors during multiple charging and discharging process.

From the above literature, it has been observed that most of the reduced switch MLI topologies have either used a greater number of isolated DC sources or used an additional H-bridge. These factors increase the inverter TSV, which may be restricted to their practical applications to lower voltage levels only. On the other hand, most of the SC-MLIs have used a smaller number of DC sources to obtain a greater number of voltage levels. However, most of the SC-MLI are normally based on symmetrical sources that realised with multiple capacitors and used a large number of switches as well as driver circuits for balancing the charging/discharging of the capacitors, which make the inverters lossy and complex for higher voltage levels. Moreover, the TSV, conduction loss, voltage stress on the highest voltage rated switches of the SC-MLIs are high. Hence their cost goes comparatively higher for increased voltage levels. Therefore, the motivation of this paper is to design an optimal generalised multi-unit MLI(MU-MLI) to minimise the required components count, proper utilisation of input DC sources and maintain the lower total standing voltage (TSV) with the increase in voltage levels.

2. Proposed CS-MLI configuration1

In this work, a crossed-switch hybrid multilevel inverter(CS-HMLI) configuration is proposed, which consists of a lesser number of switchesand isolated DC sources, as shown in

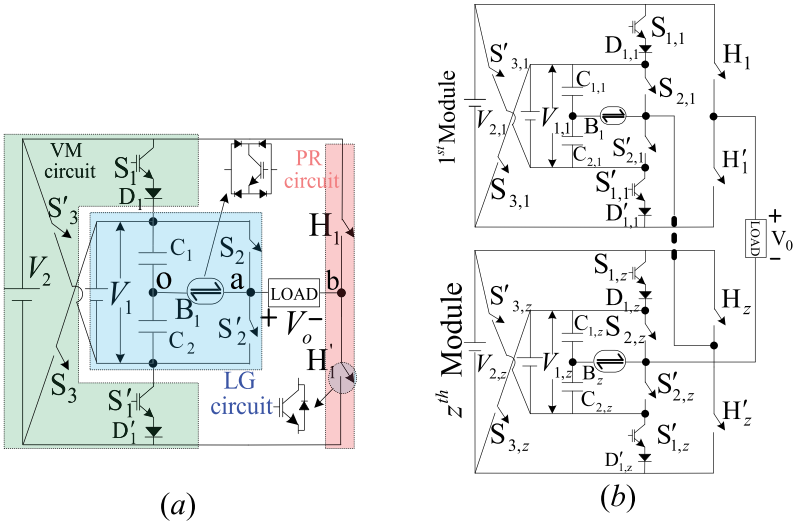

Figure 1. Proposed crossed-switch hybrid MLI (a) basic 15- level CS-HMLI module, (b) cascaded generalized module.

Figure 1(a). The important features of theproposed CS-HMLI are that the inverter has a lower number of switching devices,smaller isolated DC sources with better voltage utilization as the outputvoltage levels are obtained by all additive and subtractive combinations of thesources. Moreover, the number of conducting switches, as well as the invertertotal standing voltage (TSV) is also less. The proposed basic 15-level CS-MLIis shown in Figure 1 that consists of a level generating (LG) circuit, a voltagemultiplier (VM) circuit and a polarity reversal (PR) half-bridge. In the LGcircuit, a single isolated DC source V_1hasused that split into two equal voltages using two equal capacitors (C_1,C_2). Moreover, two unidirectional switches (S_2, S'_2)and a bidirectional switch (B_1) are used in the LG circuit, whichobtained three voltage levels across the inverter pole (i.e. $V_{ao}=\pm V_1$ and 0).On the other hand, the voltage multiplier (VM) circuit that consists of anadditional isolated voltage source V_2along with a pair of switch-diode combinations (S_1, D_1),(S'_1, D'_1) and two crossed switches (S_3, S'_3).The diode in the switch-diode is required to avoid the short-circuiting of thecapacitors (C_1& C_2) during conductions of switches $S_3$and S'_3, respectively. The VM circuit in association with thecrossed switches boosts up the voltage levels generated by the LG circuit byapproximately three times.

The polarity reversal (PR) circuit consists of two unidirectional switches (H_1, H'_1) connected across the load to alter the levels obtained by the LG circuit in association with the VM circuit to generate AC voltage. By addition and subtraction of DC source, V_2 and two capacitor voltages ($V_{c1}= V_{c2} = V_1/2$) using the switches (H_1, H'_1), (S_2, S'_2),(S_1, D_1) and S'_3 the proposed circuit can generate seven positive voltage levels like (V_2+V_1), (V_2+V_1 /2), V_2, (V_2-V_1/2), (V_2-V_1), V_1, V_1/2. Whereas, with the help of the switches (H_1, H'_1), (S_2, S'_2), (S'_1, D'_1) and S_3 the inverter converts the positive levels to the respective negative voltage levels. In this way, the proposed basic crossed-switch hybrid multilevel inverter (CS-HMLI) generates 15 voltage levels.

The switching states and the corresponding output voltage generations by the proposed CS-HMLI for the DC link voltages $V_1 = 2V_{DC}$ and $V_2 = 5V_{DC}$ are shown in Table 1. Moreover, the capacitor charging/discharging status of the proposed 15-level inverter under different switching states is also depicted in Table 1.

From Table 1, it is observed that under switching State = 1, when the switches S_2, S'_3 and H'_1 are ON, a voltage equal to $7V_{DC}$ is produced across the output for a given DC voltages $V_1 = 2V_{DC}$ and $V_2 = 5V_{DC}$. The charging/discharging state of the capacitors C_1 and C_2 are not changing (NC) under this state. Whereas, under State = 2, the capacitor C_1 charges (C) and C_2 discharges (D) due to the conduction of switches S'_3, B_1 and H_1' to obtain the voltage level $6V_{DC}$.

Similarly, under State = 4, the capacitor C_1 charges (C) and C_2 discharges (D) due to the conduction of switches S_1, B_1 and H_1' to obtain the voltage level $4V_{DC}$. In the same way, the capacitors charging and discharging status for all the switching states are depicted in Table 1. It is also observed from Table 1 that the two capacitors (C_1 and C_2) can be charged and discharged in an equal number of instants (2 instants) but in opposite manners over a complete fundamental cycle, which can ensure the capacitors self-balancing. Moreover, it is interesting to observe from Table 1 that only three switches conduct at a time each one from the LG circuit, VM circuit and PR circuit respectively to produce any of the 15 voltage levels. Thus, the conduction loss is smaller as compared to other reduced component 15-level inverters. The detailed capacitors charging/discharging paths under different switching states are presented in Figure 2. It is observed from Figure 2 and from

Table 1. The switching states and the capacitor voltage status of the 15-level inverter circuit with $V_1 = 2V_{DC}$ & $V_2 = 5V_{DC}$.

	Switching status of the MLI switches (1=ON, 0=OFF)									Capacitor states (C=charging with current i_c, D=discharging with current I_o-i_c, NC=no change)		Load Voltage (V)	Magnitude of Voltage (V)
	VM Circuit				LG Circuit			PR Circuit					
States	S_1	S'_1	S_3	S'_3	S_2	S'_2	B_1	H_1	H_1'	Capacitor C_1	Capacitor C_2		
1	0	0	0	1	1	0	0	0	1	NC	NC	(V_2+V_1)	$7V_{DC}$
2	0	0	0	1	0	0	1	0	1	C (i_c)	D (I_o-i_c)	$(V_2+0.5V_1)$	$6V_{DC}$
3	1	0	0	0	1	0	0	0	1	NC	NC	V_2	$5V_{DC}$
4	1	0	0	0	0	0	1	0	1	C (i_c)	D (I_o-i_c)	$(V_2-0.5V_1)$	$4V_{DC}$
5	1	0	0	0	0	1	0	0	1	NC	NC	(V_2-V_1)	$3V_{DC}$
6	0	0	0	1	1	0	0	1	0	NC	NC	V_1	$2V_{DC}$
7	0	0	0	1	0	0	1	1	0	C(i_c)	D(I_o-i_c)	$0.5V_1$	$1V_{DC}$
8	0	0	1	0	1	0	0	0	1	NC	NC	0	0
9	0	0	1	0	0	0	1	0	1	D(I_o-i_c)	C(i_c)	$-0.5V_1$	$-1V_{DC}$
10	0	1	1	0	0	0	0	0	1	NC	NC	$-V_1$	$-2V_{DC}$
11	0	0	0	0	1	1	0	1	0	NC	NC	$-(V_2-V_1)$	$-3V_{DC}$
12	0	0	0	0	0	1	1	1	0	D (I_o-i_c)	C (i_c)	$-(V_2-0.5V_1)$	$-4V_{DC}$
13	0	1	0	0	0	1	0	1	0	NC	NC	$-V_2$	$-5V_{DC}$
14	0	0	1	0	0	0	1	1	0	D (I_o-i_c)	C (i_c)	$-(V_2+0.5V_1)$	$-6V_{DC}$
15	0	1	1	0	0	0	0	1	0	NC	NC	$-(V_2+V_1)$	$-7V_{DC}$

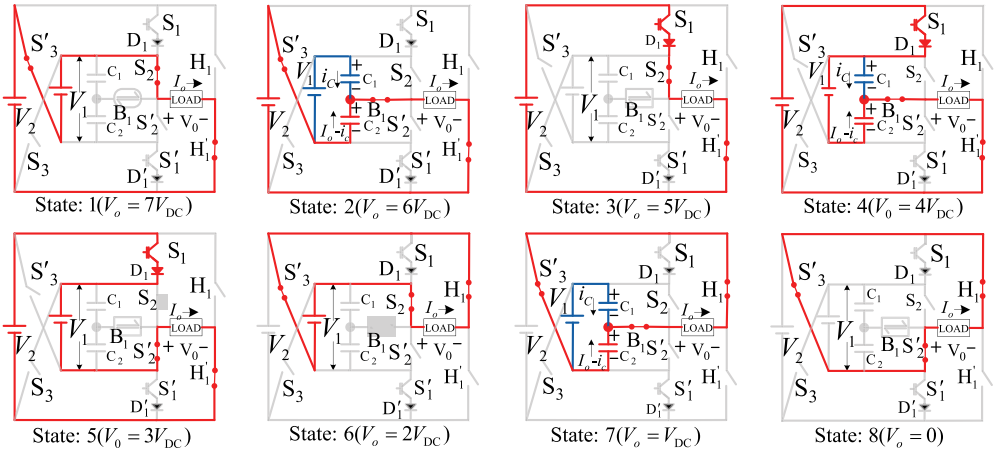

Figure 2. Current flow diagram of the proposed basic 15-level inverter under different.

Table 1 that the switches S_2, $S'_3$and H'_1 are conducted to obtain the voltage level V_o =+$7V_{DC}$ under switching state 1. Under this state, no capacitors are charged/discharged as the sum of the voltages of capacitors $C_1$and $C_2$are equal to V_1 (i.e V_{c1}+V_{c2}=V_1) and hence no change (NC) in the capacitors voltage. Under switching state 2, switches S'_3, $B_1$and H'_1 are conducted to generate the voltage level V_o=+$6V_{DC}$. Here, the capacitor C_2 discharges (D) along with the source voltage V_2 to obtain load current (I_0) flowing in the positive direction and hence the capacitor voltage decreases. However, the capacitor C_1 charges under this state and the voltage across the capacitor C_1 increases. The charging current that circulates through C_1 is i_C and the discharging current through the C_2 is I_o– i_c respectively. Similarly, the charging and discharging states of the two capacitor and

current path under different positive states are depicted in Table 1 as well as in Figure 2. It is observed from Table 1 and Figure 2 that, during positive half-cycle, the capacitor C_1 charges thrice with a current i_c. Whereas, the capacitor C_2 discharges thrice with a current ($I_0 - i_c$) and behaves opposite to the capacitor C_1. The reverse will happen during the negative half-cycle. The charging/discharging characteristics of the capacitors C_1 and C_2 are depicted graphically by the simulation waveforms of capacitor voltages as represented in Section 7 (Figure 6).

3. Operation of an extended 27-level inverter

An extended single module, 27-level inverter of the proposed cross-switched hybrid MLI (CS-HMLI) configuration is shown in Figure 3. Similar to the basic 15-level CS-HMLI, the extended 27-level inverter is also having three parts like level generating (LG) circuit, voltage multiplier (VM) circuit and polarity reversal (PR) circuit as shown in Figure 3. The circuit is consisting of three DC sources (V_1, V_2 & V_3), eight unidirectional switches like the basic 15-level CS-HMLI, three bi-directional switches (B_1, B_2 & B_3) and four capacitors (C_1, C_2, C_3 & C_4). The magnitude of the DC sources are selected in the ratio of 2:4:9 (i.eV_1:V_2:V_3 = $2V_{DC}$:$4V_{DC}$:$9V_{DC}$) to obtain 27 voltage levels. The voltage source V_1 is split into two equal voltages using two equal capacitors (C_1& C_2). Moreover, two more capacitors of equal capacitance (C_3 & C_4) are introduced in the extended circuit, which maintain the equal voltages across all the capacitors (C_1, C_2, C_3 & C_4). Thus, with one additional voltage source V_2 with two capacitors along with two bidirectional switches in the LG circuit one can extend the proposed 15-level inverter to a 27-level inverter as shown in Figure 3. The detailed operation of the 27-level inverter and the corresponding charging/discharging states of the capacitors are explained schematically in Figure 4 under different switching states. The operation of this 27-level inverter is similar to the proposed basic 15-level CS-HMLI. Still, in order to explain the charging/discharging characteristics of the four capacitors of the extended 27-level inverter for getting different positive voltage levels, its

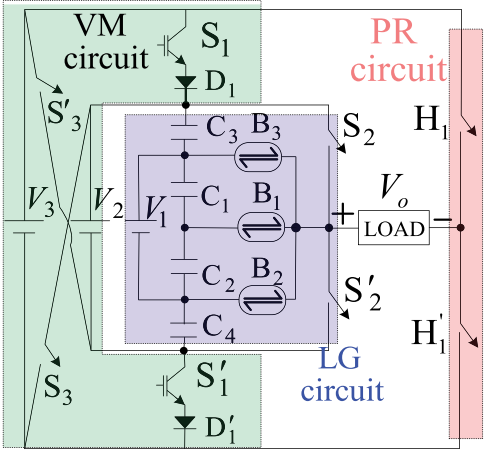

Figure 3. Extended 27-level inverter of the proposed CS-HMLI with ratio of DC-link voltages (V_1:V_2 :V_3 = $2V_{DC}$: $4V_{DC}$: $9V_{DC}$).

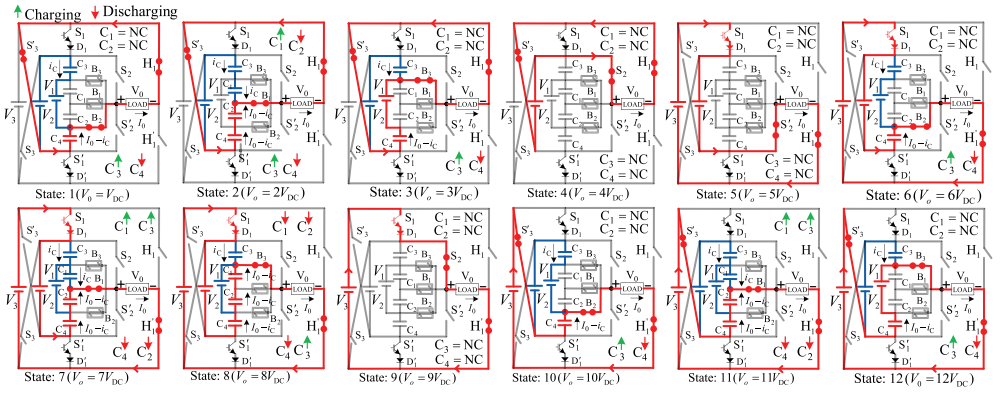

Figure 4. Modes of operation of the proposed 27-level inverter configuration.

schematic circuit diagram under different states have been drawn in Figure 4. Moreover, to indicate the charging and discharging of any capacitors (i.e C = charging, D = discharging), symbolically an upward green arrow (↑) and downward red arrow (↓) is used respectively.

For switching state 1, to obtain voltage level $V_o = V_{DC}$, the switching devices S'_3, B_2 and H_1 are to be conducted, which discharge the capacitor C_4 and charge the capacitor C_3 as shown in Figure 4. Under this state, the states of the capacitors $C_1$and C_2 are not changing (NC) as the sum of the voltage across them is equal to V_1. Similarly, under switching state 2, capacitors C_4&C_2 are discharged to the current (I_o-i_c) whereas, the capacitors C_1 & C_3 are charged to the current (i_c). In this way, the charging/discharging of all the capacitors and the current paths under all the positive switching states are presented graphically in Figure 4. It is observed from Figure 4 that capacitor C_1 charges under three states (state: 2, 7 & 11) in the positive half-cycle during which the capacitors C_2 is discharged so that the total sum of their voltages remained equal to V_1 (i.e. v_{c1}+ v_{c2}=V_1). Similarly, the capacitor C_3 charges under nine states (Figure 4) during which the capacitor C_4 discharges in such a manner that the sum of voltages across them always remained equal to V_2-V_1 (i.e. v_{c3}+ v_{c4}= V_2-V_1). The reverse may be happened in the negative half cycle, which is graphically illustrated in Figure 7 in their charging/discharging current waveforms.

4. Proposed generalised expression of the cascaded multi-unit (MU-MLI)

For high-power applications, a generalised cascaded asymmetrical MLI can be designed using 'z' number of proposed 15-level CS-MLI modules as shown in Figure 1(b). The z^{th} CS-MLI module in the generalised cascaded MLI as shown in Figure 1(b) contains one bi-directional switches (B_z), three complementary unidirectional switch-pairs ($S_{2,z}$, $S'_{2,z}$), ($S_{3,z}$, $S'_{3,z}$), (H_z, H'_z) and two complementary switch-diode pairs ($S_{1,z}$, $D_{1,z}$) & ($S'_{1,z}$, $D'_{1,z}$) to obtain fifteen voltage levels across the module. Moreover, two isolated voltage sources ($V_{1,z}$ &$V_{2,z}$) are used that are added and subtracted to obtain the 15 voltage levels that ensure full utilisation of the sources. For the proposed generalised cascaded MLI with a maximum output voltage (V_{omax}), the magnitude of the two DC voltages ($V_{1,z}$ & $V_{2,z}$) of the z^{th} inverter module are:

$$V_{1,z} = 2 \times 15^{z-1} \times \frac{2V_{o\max}}{N_L - 1} \tag{1}$$

$$V_{2,z} = 5 \times 15^{z-1} \times \frac{2V_{o\max}}{N_L - 1} \tag{2}$$

Where, N_L is the number of voltage levels obtained by the generalised cascaded inverter having z number of 15-level modules is derived as:

$$N_L = 15^z \tag{3}$$

Further, for a given inverter output voltage V_{omax} having voltage levels N_L, the magnitude of step voltage V_{DC} can be expressed as:

$$V_{DC} = \frac{2V_{o\max}}{N_L - 1} \tag{4}$$

If $V_{omax,z}$ is the maximum voltage across the z^{th} inverter module, the maximum sum of voltage of the individual unit is the V_{0max} across the cascaded multi-unit MLI.

5. Comparison of the proposed CS-HMLI with similar MLIs developed recently

In terms of capacitors (N_C) as well as DC voltages (N_{DC}), the proposed generalised cascaded CS-HMLI topology also better as compared to the other similar MLI configurations having voltage source and capacitors as depicted in Figure 5(c,d). Moreover, in terms of TSV/V_{DC}, the proposed MLI is also better for a given voltage level as compared to most of the other similar kinds of MLIs reported here except topologies given in Gautam (2018), Samadaei and Adabi (2018), and Saeedian et al. (2019), as depicted in Figure 5(d). Therefore, in terms of N_{sw}, N_{DC}, N_C and inverter TSV, the proposed CS-HMLI topology is much better than the others, which indicated that the cost of the proposed MLI should be lower than the most of the other MLI topologies. As the cost of an inverter mainly depends upon the major inverter components like N_{sw}, the number of driver circuits ($N_{Driv.}$), N_C, N_{DC} and TSV per unit ($TSV_{P.U}$), etc. A cost function (CF) for the proposed MLI, which depends upon the number of components is expressed using the concept developed in Pal et al. (2022) as:

$$CF = (N_{sw} + N_{driver} + N_C + \beta \times TSV_{PU}) \times N_{DC} \tag{5}$$

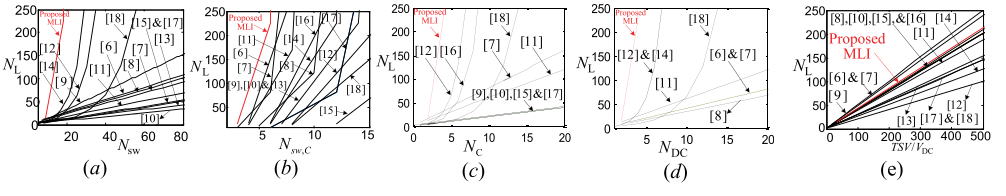

Figure 5. Performance of the proposed MLI compared to the other recent MLIs for various voltage levels (N_L) (a) the number of switches (N_{sw}), (b) the number of conducting switches ($N_{sw,c}$), (c) the number of Capacitors (N_C), (d) number of DC sources (N_{DC}) and (e) Total standing voltage (TSV).

In the same way, the cost function of the other recently developed MLIs reported here also derived for the comparison purpose as given in Table 2. For a case study, the per-unit value of cost function for some of the existing 15-level inverter is calculated as presented in Table 2 and compared with the proposed 15-level CS-HMLI at identical rating. It has been observed in Table 2 that the proposed 15-level inverter has the lowest CF compared to the other 15-level MLIs reported here. For higher voltage levels, the value of CF/N_L can be much better than the other topologies. In the same way, the cost function of the other recently developed MLIs reported here also derived for the comparison purpose as given in Table 2.

For a case study, the per-unit value of cost function for some of the existing 15-level inverter is calculated as presented in Table 2 and compared with the proposed 15-level CS-HMLI at identical rating. It has been observed in Table 2 that the proposed 15-level inverter has the lowest CF compared to the other 15-level MLIs reported here. For higher voltage levels, the value of CF/N_L can be much better than the other topologies.

In addition to the number of components, the cost of the inverter, which also depends upon the cost of the individual components. In order to compare the cost of the proposed 15-level CS-HMLI with the other similar multilevel inverters (Babaei et al., 2015; Gautam, 2018; Jayabalan et al., 2017; Liu et al., 2018; Majumdar et al., 2020; Paul et al., 2021) of the same inverter rating having multiple DC sources, their detailed industrial components cost is considered here. The unit cost of a standard dc power source supplying to the inverter DC link of 100 V, 3A rating available from Keysight (N6776A) is assumed as $2325.40. Similarly, the unit cost of the capacitors of rating 400 V, 4700μF, from Alcon Electronics is considered as $21. The unit cost of a power diode rated at 600 V, 15A product from Mouser Electronics (MUR1560 G), is $1.13. In addition, the unit cost of one standard gate driver from Semikron (Skyper 32 R) of rating 14.4 V–15.6 V&15A and an IGBT of 900 V, 60A from MITSUBISHI (CT60AM-18F) are available at the cost of $175.84 and $2.68 respectively. Based on the price of the individual components, the overall approximate cost of all the 15-level inverters having multiple DC sources is tabulated in Table 3. It is observed from Table 3 that the industrial cost of the proposed 15-level inverter is much lesser compared to the industrial cost of the other recently developed inverters having multiple DC sources.

6. Simulation and experimental verification of the proposed 15-level and the 27-level inverter

To show the performance of the proposed basec15-level CS-HMLI (Figure 1(b)) and an extended 27-level inverter (Figure 3), both the simulation and experiments are conducted. Among the various available pulse generation techniques, the nearest level control (NLC) technique (Pal et al., 2022) is adopted for the proposed inverters to obtain the lower switching losses. For simulation and experimental purposes, the magnitude of input DC voltages for the basic 15-level inverter is considered as $V_1 = 60$ V and $V_2 = 150$ V and for 27-level extended inverter $V_1 = 20$ V, $V_2 = 40$ V and $V_3 = 90$ V, respectively, under R-L load (R = 75Ω and L = 50mH). These DC voltages are realised by a multi-winding transformer and rectifier with smoothing capacitors arrangements due to their availability in the laboratory. Figure 6 depicts the experimental arrangements of the proposed 15-level/27-levelcross switched hybrid MLI (CS-HMLI) that is designed with IGBTs (CT60AM-18F) and

Table 2. The value of cost function per number of voltage levels (CF/N_L) of the proposed 15-level CS-HMLI-based generalised inverters with other similar MLI topologies and the proposed 27-level extended CS-HMLI.

MLI Structures	Samadaei and Adabi (2018)	Gautam (2018)	Saeedian et al. (2019)	Gautam (2018)	Majumdar et al. (2020)	Khan et al. (2020)	Khenar et al. (2018)	Proposed generalized cascaded MLI	Proposed 27-level extended CS-HMLI (z=1)
N_L	16z+1	8z+1	$2^{z+1}+1$	$2^{z+1}-1$	9^z	2z+1	2z+1	15^z	27
N_{SW}	12z	7z	z+4	5z	4z+1	3z+2	3z+5	9z	14
$N_{SW,C}$	4z	3z	2z	2z	4z	3z	4z	3z	3
$N_{Cap.}$	–	z	2z	z	–	z	z	2z	4
N_{DC}	4z	2z	1	z	z	1	1	2z	3
$N_{Driv.}$	9z	7z	z+4	z	4z+1	3z+2	3z+5	9z	11
N_{Diode}	–	4z	2z	4z	-	-	2z	4z	2
TSV/$V_{0,max}$	5	4.3	4	9.1	4.7	4.9	6.7	5	5.3
CF/N_L (β=0.5)	5.5	7.5	4.1	12.9	5.6	3.8	4.1	3.0	3.5
CF/N_L (β=1.5)	6.7	8.5	5.0	15.4	6.6	4.0	4.6	3.6	4.1

Table 3. Industrial cost comparison of the recent MLIs with multiple DC sources.

Topology	N_L	N_{sw}	N_{Driver}	N_{DC}	$N_{Cap.}$	N_{Diode}	Total cost ($)
Gautam (2018)	15	20	20	4	4	16	12,974.08
Majumdar et al. (2020)	15	17	17	4	0	0	12,336.44
Paul et al. (2021)	15	12	12	3	–	–	9118.44
Babaei et al. (2015)	15	16	16	7	–	–	19,134.12
Jayabalan et al. (2017)	15	10	10	4	–	–	11,086.80
Liu et al. (2018)	15	14	13	4	–	–	11,625.04
Proposed	15	9	9	2	–	4	6262.00

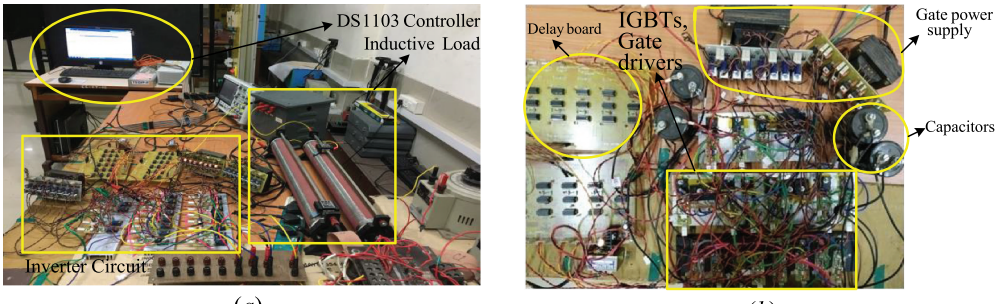

Figure 6. Laboratory prototype of the 15-L/27-L inverter (a) Total experimental setup including DS1103 controller box, inductive load, inverter circuit and power supply, (b) detailed inverter circuit consisting IGBTs and gate drivers, gate power supply, delay board and capacitors.

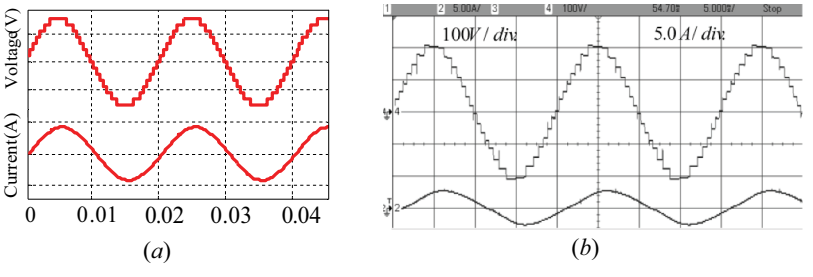

Figure 7. Results of the 15-level inverter at M_i=1.0 (a) Simulation result, (b) Experimental validation.

ultrafast diodes (MUR1560 G) with Opto-Isolators (TLP250) based driver circuit of 2.0 kW inverter rating. The magnitude of all the capacitors used for the proposed inverters (C_1, C_2, C_3 & C_4) are considered as 2200 µF, 400 V. The NLC based control algorithm for the proposed CS-HMLIs (15-level/27-level) are implemented using DS1103 based digital controller due to its availability in the laboratory.

Figure 7 depicts the simulation and the corresponding experimental results of the proposed basic15-level CS-HMLI at modulation index (M_i) = 1.0 for an R-L load (R = 75Ω & L = 133mH) under steady state condition. It is observed that, 15 distinct voltage steps are obtained at the output, which results in nearly sinusoidal load current in both simulation & experimental results.

To demonstrate the dynamic behaviour of the proposed 15-level inverter, the waveforms of inverter voltage and current under different modulation indices (M_i) and the dynamic load variations are presented in Figure 8(a,b), respectively. It has been observed from Figure 8(a) that with the variation of modulation index (M_i) from 1.0 to 0.25, the inverter output voltage levels for a constant load with R = 75Ω & L = 133mH are reduces from 15 to 3 levels, which results a gradual change in load current from 2783A to 0.3A in accordance with the voltage changes. Whereas, for dynamic variation of load resistance from R = 75Ω to R = 141Ω with L = 133mH at a constant M_i = 1.0, keeping the inverter voltage fixed at 15 levels, the output RMS current smoothly decreases from I = 2.783A to I = 1.49A in accordance with the load variations.

The input DC source V_1 is split into two capacitors C_1 and C_2, individual capacitors are charged to almost equal voltage magnitude of $V_1/2$. The experimental ripple voltage waveform of both the capacitors C_1 and C_2 are depicted in Figure 9 which are denoted by V_{C1} and V_{C2}. For the proposed 15-level inverter, the voltage waveform of capacitors C_1 and C_2 represent that they are self-balanced under steady state.

In addition, the magnitude of currents delivered by the voltage source V_2 and the input source V_1 is split by two capacitors C_1 and C_2 are measured experimentally in Figure 10. The current delivered by the input DC source V_2 as I_2 as shown in Figure 10(a) and the charging and discharging current of two capacitors C_1 and C_2 are termed as I_{C1} and I_{C2} are depicted in Figure 10(b,c) respectively. It is observed that the inrush current absorbed by

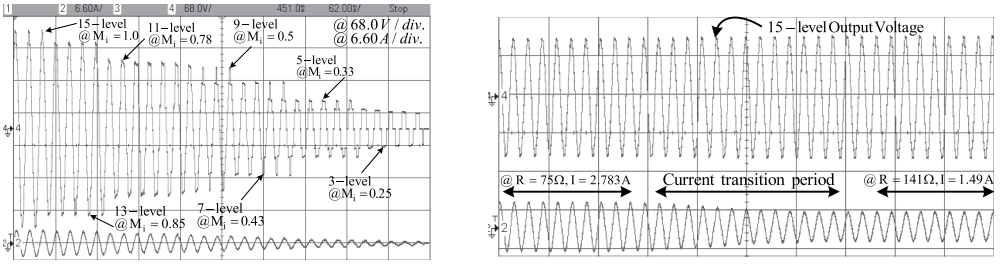

Figure 8. Dynamic response of output voltage and current of the proposed 15-level inverter under (a) variation in M_i, (b) variation with load impedance.

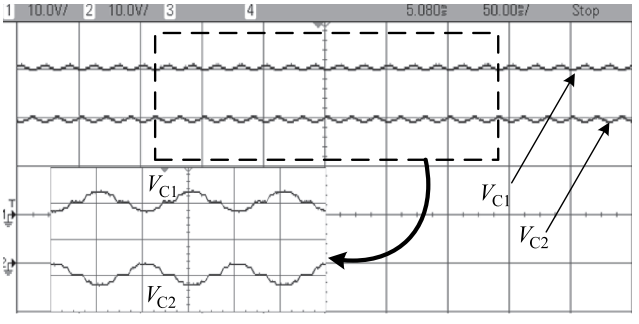

Figure 9. The experimental voltage waveform of both the capacitors C_1 and C_2.

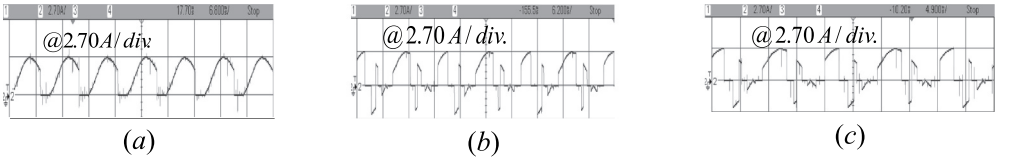

Figure 10. Experimental waveform of input currents (a) I_2, (b) I_{C1}, and (c) I_{C2}.

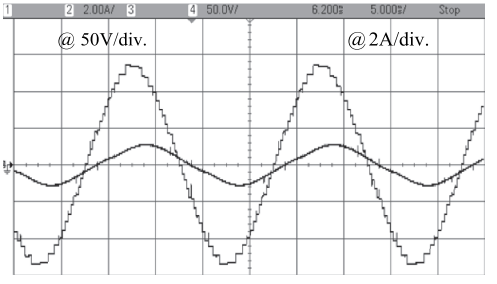

Figure 11. Experimental results of output voltage and current of the 27-level inverter at M_i=1.0.

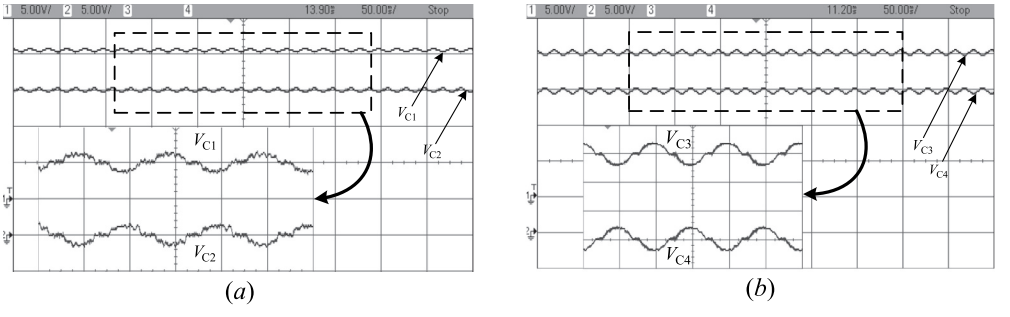

Figure 12. Steady state voltage ripple of the capacitors (a) C_1 and C_2 with voltage value of V_{C1} and V_{C2}, (b) C_3 and C_4 with voltage value of V_{C3} and V_{C4}.

the capacitors of the proposed 15-level inverter is much lower compared to the capacitors used by the switched capacitor MLIs.

In addition, the proposed 27-level inverter unit using three DC sources, four capacitors and eleven switches is implemented in the laboratory having DC link voltages (V_0, V_1 and V_2) of magnitude 20, 40 and 90 volts (in the ratio 2:4:9) as given in Equation (5–7). The Figure 11 depicts the output voltage and current of the 27-level inverter for R-L load having a magnitude of $R = 133\Omega$ and $L = 100$ mH, respectively.

Figure 12(a,b) schematically explains the steady state voltage across the capacitors C_3, C_1, C_2 and C_4. It is observed that after transient state the capacitor voltage gets automatically balanced without the requirement of any extra control circuit arrangement.

The efficiency of the proposed 15-level inverter is calculated (Pal et al., 2022) considering the inverter is delivering the output power of 434.7 W at 50 Hz. The losses of the inverter such as switching loss, conduction loss and capacitor voltage ripple loss are

calculated as 0.054 W, 12.9 W and 6.7 W respectively. Therefore, the efficiency of the proposed 15-level inverter is calculated as 95.7% using the NLC technique.

7. Conclusions

A new MLI topology is developed and presented in this work that generates maximum number of output voltage levels utilising minimum components and lower total standing voltage. A basic 15-level topology has been designed that necessitates a voltage multiplier circuit in association with LG unit to multiply the voltage levels thrice at the output due to the addition and subtraction of input DC sources and capacitors. In addition, a 27-level inverter is developed using three DC sources and four capacitors. It is observed that the capacitors are well balanced. From the comparative analysis of the proposed MLI with the existing topologies, the superiority of the proposed MLI in terms of the number of inverter switches and the capacitors utilised are proven. Moreover, the study of inverter cost from the cost function analysis is also better than most of the topologies for a given voltage level. The proposed 15-level and 27-level inverter is experimentally validated using DS1103 based digital controller that proven its physical implication.

Disclosure statement

No potential conflict of interest was reported by the authors.

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